

10

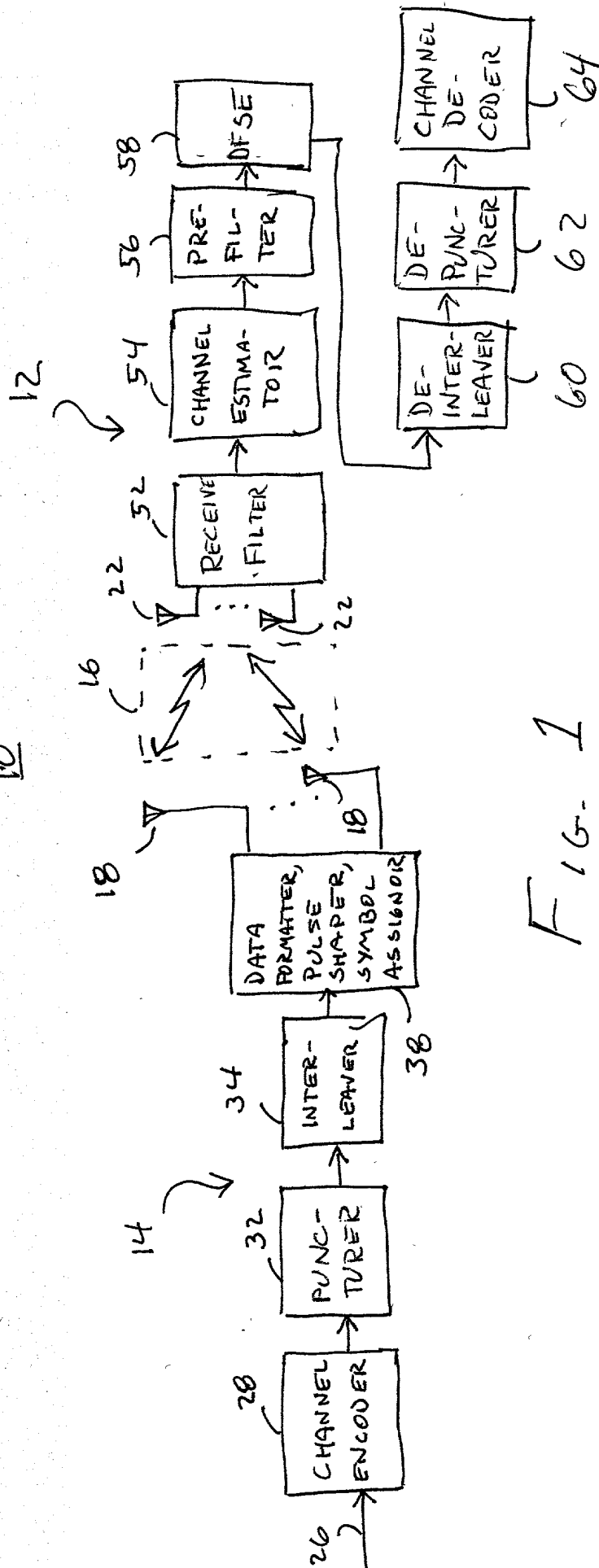


FIG. 1

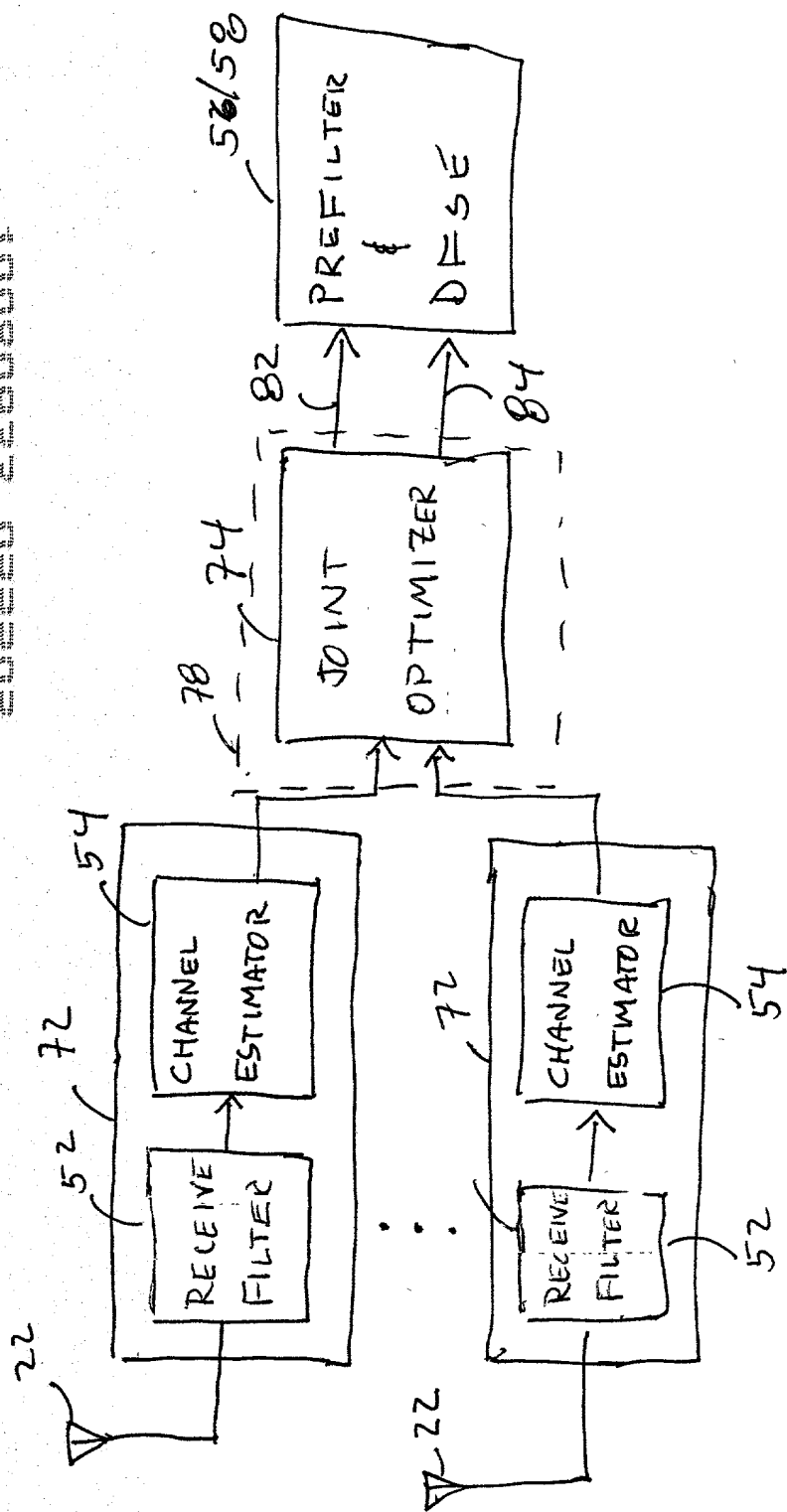


Fig. 2

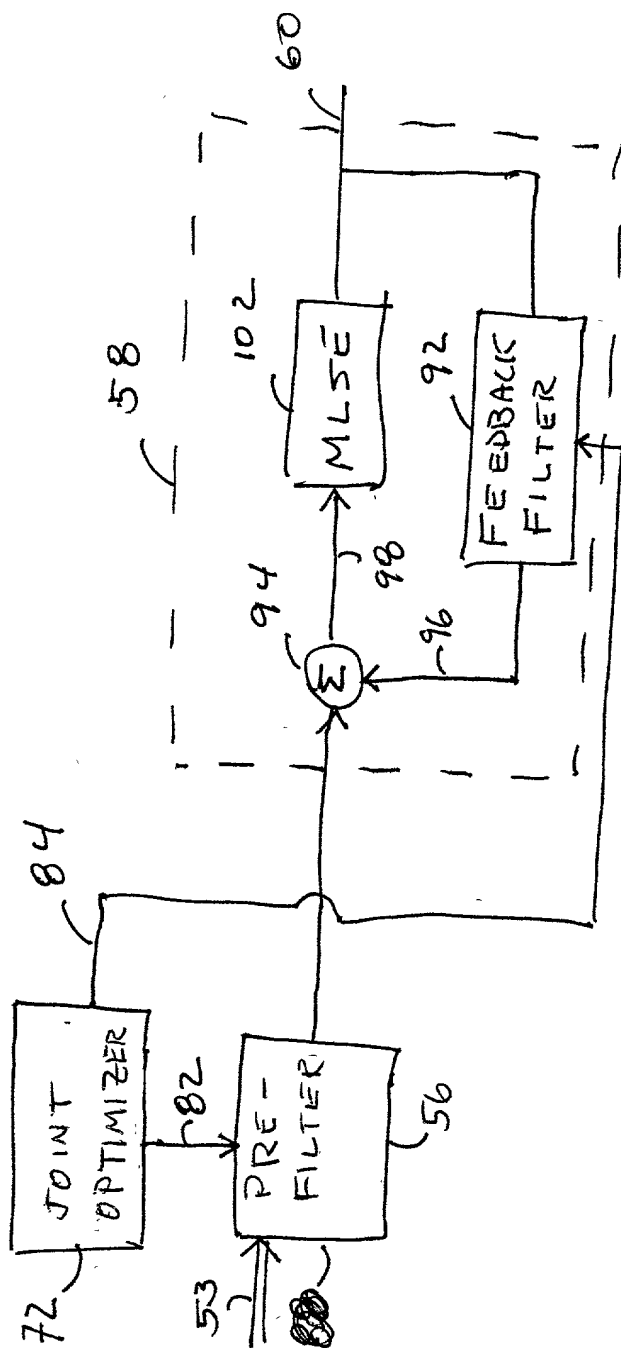


FIG. 3

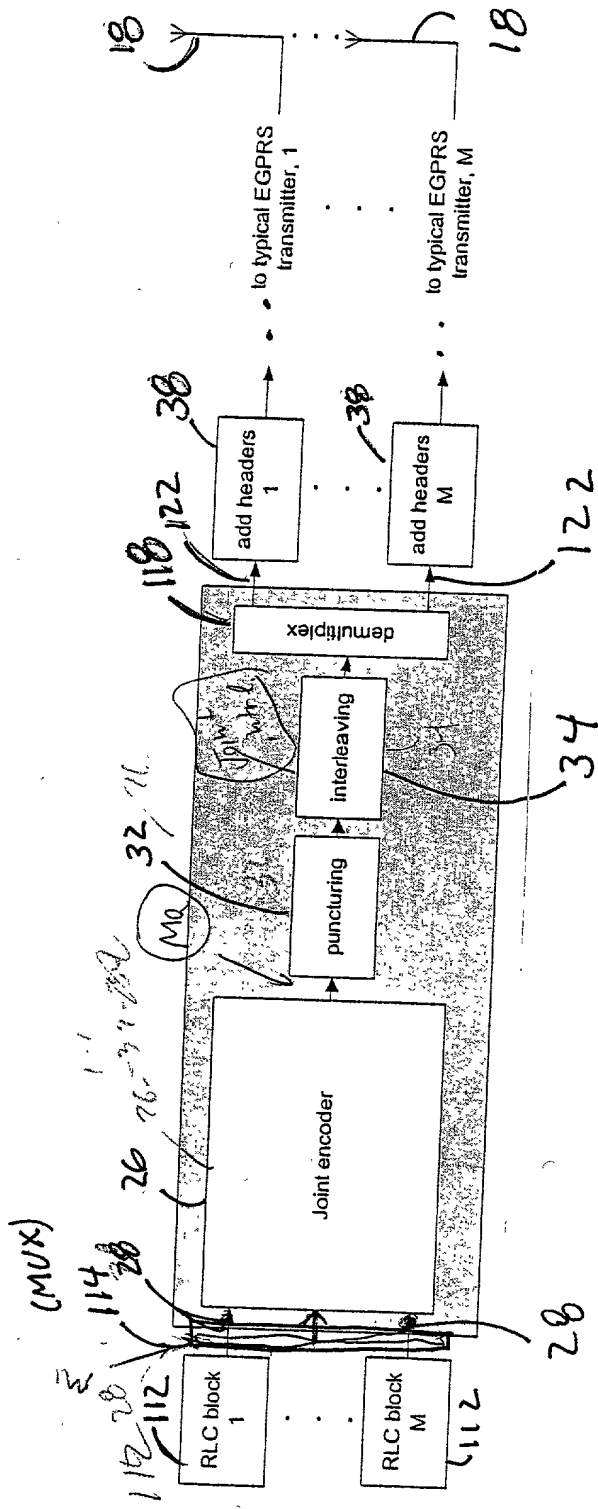


FIG. 4

FIG. 5 is a block diagram of a receiver system. The system includes two parallel processing paths. Each path starts with a Receive Filter (122) receiving an input signal (22). The filtered signals (124) are then processed by a Space-Time Prefilter (126). The outputs of the Space-Time Prefilters (128) are fed into a Joint Channel estimator (130). The Joint Channel estimator (130) provides feedback to the Space-Time Prefilters (126). The outputs of the Space-Time Prefilters (128) are then processed by SISO Equalizers (132). The outputs of the SISO Equalizers (134) are fed into a Multiplex (136). The Multiplex (136) outputs a signal (138) to a Joint Turbo Decoder (140). The Joint Turbo Decoder (140) outputs a signal (142) to a Remove tail bits block (144). The Remove tail bits block (144) outputs a signal (146) to a De-Multiplex block (148). The De-Multiplex block (148) outputs two signals (150 and 152), each labeled as 462 bits.

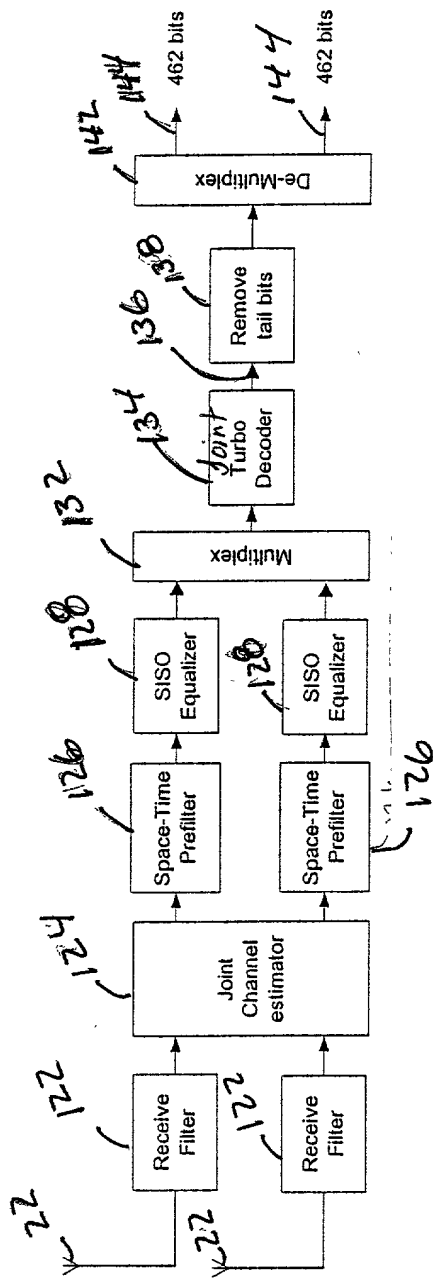


FIG. 5

152

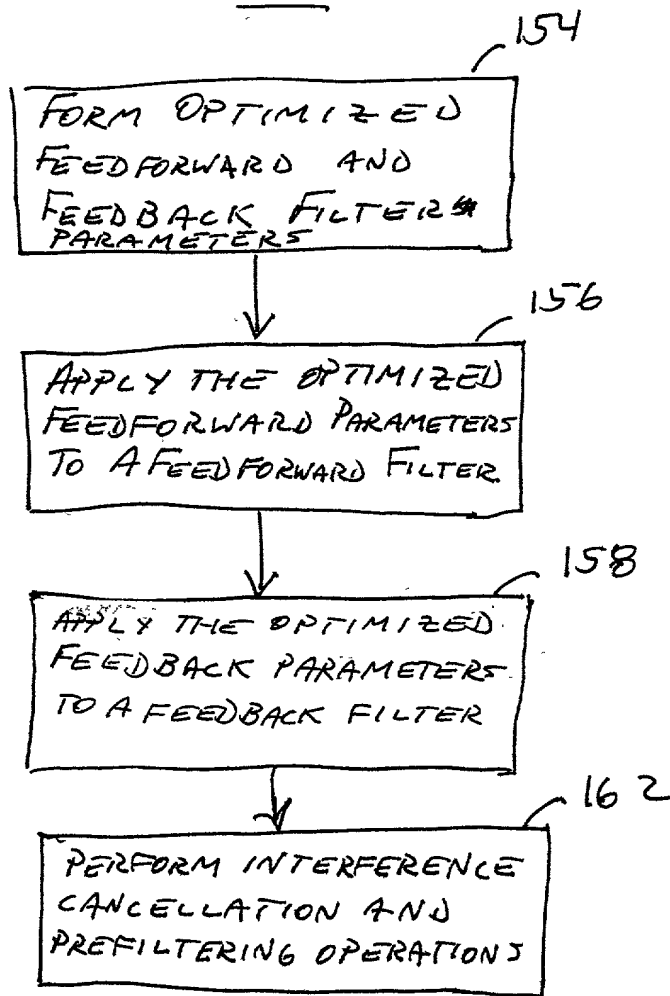


FIG. 6